a bit line coupled to one end of said NAND-cell unit;

a program circuit, coupled to said word lines and said bit line, for applying a write voltage to the word line of a selected memory cell, for applying a verify voltage to the word line of the selected memory cell to determine an actual threshold voltage of the selected memory cell while applying a pass voltage to remaining word lines of unselected memory cells in said NAND-cell unit to make the unselected memory cells act as transfer transistors, for applying a first level voltage to the bit line to change the threshold voltage of the selected memory cell in which it has been determined that the threshold voltage has not reached a given threshold voltage level, said first level voltage being combined with said write voltage, and for applying a second level voltage to the bit line to maintain the threshold voltage of the selected memory cell in which it has been determined that the threshold voltage has reached said given threshold voltage level, said second level voltage being combined with said write voltage;

wherein said pass voltage is higher than said verify voltage.

133. (Amended) A multi-level nonvolatile semiconductor memory device comprising:

a NAND-cell unit including a plurality of memory cells connected in series, each of said memory cells including a transistor with a control gate and a charge storage portion and having storage states of at least three threshold voltage levels;

a plurality of word lines connected to respective control gates;

a bit line coupled to one end of said NAND-cell unit;

a read circuit, coupled to said word lines and said bit line, for applying one of at least two read voltages to the word line of a selected memory cell to determine whether or not a

threshold voltage of the selected memory cell is higher than said one of at least two read voltages while applying a pass voltage to remaining word lines of unselected memory cells in said NAND-cell unit to make the unselected memory cells act as transfer transistors;

wherein said pass voltage is higher than said at least two read voltages.

139. (Amended) A multi-level nonvolatile semiconductor memory device comprising:

a NAND-cell unit including a plurality of memory cells connected in series, each of said memory cells including a transistor with a control gate and a charge storage portion and having storage states of at least three threshold voltage levels;

a plurality of word lines connected to respective control gates;

a bit line coupled to one end of said NAND-cell unit;

a verify circuit, coupled to said word lines and said bit line, for applying one of at least two verify voltages to the word line of a selected memory cell to determine whether or not a threshold voltage of the selected memory cell reaches one of said at least three threshold voltage levels while applying a pass voltage to remaining word lines of unselected memory cells in said NAND-cell unit to make the unselected memory cells act as transfer transistors;

wherein said pass voltage is higher than said at least two verify voltages.

150. (Amended) A multi-level nonvolatile semiconductor memory device comprising:

a NAND-cell; unit including a plurality of memory cells connected in series, each of said memory cells including a transistor with a control gate and a charge storage portion and having storage states of at least three threshold voltage levels;

a plurality of word lines connected to respective control gates;

a bit line coupled to one end of said NAND-cell unit;

a verify circuit, coupled to said word lines and said bit line, for applying, to the word line of a selected memory cell, a first voltage in a first portion of a verify operation and a second voltage in second portion of said verify operation while applying, to remaining word lines of unselected memory cells in said NAND-cell unit, a third voltage in said first and second portions of said verify operation.